REMARKS

The claims are claims 1 to 4, 16, 17 and 27 to 54.

The application has been further amended to present a SUMMARY OF THE INVENTION as required by the Examiner.

Claims 1, 16, 27, 30, 32 and 35 are amended. New claims 37 to 54 are added. Claims 1, 16 and 27 have been amended to delete the limitation that the number of output terminals equals the second fixed size. Claims 1, 16 and 27 are further amended to recite a data processor clock, a transmission output clock and the relationship between these quantities and the first and second fixed sizes. Claims 30, 32 and 35 are amended to change "current block register" to match the previously recited "current packet register." New claims 37, 43 and 49 recite that the transmission clock rate is greater than the data processor clock rate as described in the application at page 37, line 12 to page 38, line 4 and originally claimed in claims 7 and 18. Claims 38, 44 and 50 recite the second fixed size is greater than the first fixed size as described in the application at page 38, lines 13 to 15, illustrated in Figures 23A and 23B and originally claimed in claims 9, 12, 14, 20 and 26. Claims 39, 45 and 51 recite that the transmission clock rate is less than the data processor clock rate as originally claimed in claims 10 and 21. Claims 40, 46 and 52 recite that there is no output second information blocks in the absence of valid first information blocks as described in the application at page 40, lines 12 to 15 and illustrated in Figure 25. Claims 41, 47 and 53 recite producing a last second information block with NOP bits and thereafter stalling in the absence of valid first information blocks as described in the application at page 40, line 16 to page 41, line 4 and illustrated in Figure 26. Claims 41, 48 and 54 recite producing second information blocks with NOP bits in the absence of valid first

information blocks as described in the application at page 41, lines 5 to 11 and illustrated in Figure 27.

Claims 1 to 4, 16, 17 and 27 to 36 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The FINAL REJECTION states that "A person skilled in the art would not know how to determine the size of plurality of terminals from the provided disclosure, given the fact that the size of the second fixed size is undetermined," and "Examiner is unable to find the specification where it states that the number of terminals is the same as size of the second packet."

Claims 1, 16 and 27 have been amended to delete the recitation that the number of terminals equals the second fixed size. Accordingly, claims 1, 16 and 27 are now proper under 35 U.S.C. 112.

Claims 1 to 4, 8, 9, 15 to 17 and 27 were rejected under 35 U.S.C. 102(e) as being anticipated by Edwards, U.S. Patent No 6,732,307.

Claims 1, 16 and 27 recite subject matter not anticipated by Edwards. Claim 1 recites "collecting internal emulation information from a data processor at a data processor clock rate" and "outputting a sequence of the second information blocks via a plurality of terminals at a transmission clock rate, said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks." Claims 16 and 27 each recite similar limitations. This subject matter is disclosed in the application at page 38, lines 5 to 12. Edwards fails to disclose the recited relationship between the data sizes and the respective clock rates. Accordingly, claims 1, 16 and 27 are allowable over Edwards.

Claims 2, 17 and 34 recite subject matter not anticipated by Edwards. Claims 27, 17 and 34 each recite "said second fixed size is smaller in size than said first fixed size." The FINAL REJECTION states at page 4, lines 4 to 6:

> "Examiner respectfully disagrees as Edwards teaches fixed upper limit in size of the first information block (Col. 17 Lines 58-67 - 3*8 bytes) and second information block (Fig. 9 Limited to 8 bytes) in the trace buffer."

The Applicants respectfully submit that these two portions of Edwards in fact refer to the same limitation and not to different limitations. Edwards states at column 17, lines 45 to 52:

> "FIG. 9 shows one embodiment of a trace buffer. Trace buffer 901 may include either variable or fixed length messages, the largest size message entry 902 fitting within 3*64-bit words. In one aspect, debug circuit 103 may write trace messages into trace buffer 901 at fixed 3*64-bit intervals."

This size of "3*64-bit words" cited in the description of the trace buffer illustrated in Figure 9 is the same limitation of Edwards column 17, lines 58 to 67 cited in the FINAL REJECTION. Because these limitations upon the trace message length recited in Edwards are the same, they cannot anticipate the limitation recited in claims 2, 17 and 34 that "said second fixed size is smaller in size than said first fixed size." Accordingly, claims 2, 17 and 34 are allowable over Edwards.

The FINAL REJECTION states at page 4, lines 15 to 18:

> "Further, claims 2, 17 and 34 also suffer from not clearly defining the meets and bounds of what is meant by first fixed size and second fixed size. See 35 USC 112 rejections below."

The Applicants respectfully submit that this is in error. Recitation that two quantities have respective fixed sizes is not

indefinite. Such a limitation prohibits either the first size or the second size from being variable. Thus these limitations are not indefinite. Note further that claims 2, 17 and 34 require "said second fixed size is smaller in size than said first fixed size." This further limitation is also definite as required by 35 U.S.C. 112. Selecting a fixed first size and a fixed second size, one skilled in the art would be able to determine immediately whether the second size is smaller than the first size. The Examiner is confusing a broad limitation with an indefinite limitation. Stating that two quantities are both fixed and that one is smaller than the other is both definite but not very limiting. These limitations are definite as required by 35 U.S.C. 112 because it is possible to determine without ambiguity whether two selected quantities satisfy the limitations or not. Since there is no ambiguity in determining whether the limitation is satisfied, they are definite under 35 U.S.C.112.

Claims 30 to 36 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards U.S. U.S. Patent No. 6,732,307 and Sterbenz et al "Report and Discussion n the IEEE ComSoc TCGN Gigabit Networking Workshop 1995."

Claims 30, 32 and 35 recite subject matter not made obvious by the combination of Edwards and Sterbenz et al. Claims 30, 32 and 35 recite "said first fixed size is an integral multiple of said second fixed size." This subject matter is not disclosed in Edwards. Claims 30, 32 and 35 further recite a manner of forming the second information blocks disclosed in this application at page 38, line 20 to page 39, line 3. This subject matter is likewise not disclosed in Edwards. The FINAL REJECTION cites Sterbenz et al as disclosing this subject matter. However, the cited portions of Sterbenz et al teach neither that a first fixed size is an integral multiple of a second fixed size nor the current packet register.

Accordingly, claims 30, 32 and 35 are allowable over the combination of Edwards and Sterbenz et al.

Claims 31, 33 and 36 recite subject matter not anticipated by Edwards. Claims 31, 33 and 36 recite operation of this invention when the first fixed size is not an integral multiple of the second fixed size as described in the application at page 39, lines 4 to 19 and illustrated in Figure 22A. In particular, Edwards fails to teach the recited current packet register and last packet register recited in these claims. The FINAL REJECTION cites Sterbenz et al as disclosing this subject matter. However, the cited portions of Sterbenz et al teach neither that a first fixed size is an integral multiple of a second fixed size nor the current block register. Accordingly, claims 31, 33 and 36 are allowable over the combination of Edwards and Sterbenz et al.

New claims 37 to 54 recite subject matter not made obvious by the combination of Edwards and Sterbenz et al. Claims 37, 43 and 49 recite that the transmission clock rate is greater than the data processor clock rate. Edwards and Sterbenz et al fail to teach this subject matter. Claims 38, 44 and 50 recite that the second fixed size is greater than the first fixed size. Neither Edwards not Sterbenz et al include any teaching about relative sizes and thus cannot make this subject matter obvious. Claims 39, 45 and 51 recite that the transmission clock rate is less than the data processor clock rate. Edwards and Sterbenz et al fail to teach this subject matter. Claims 40 to 42, 46 to 48 and 52 to 54 recites various alternative operations in the absence of valid first information blocks. Neither Edwards nor Sterbenz et al make obvious this subject matter.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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